module p2(l, d);

output l;

input[2:0] d;

not not2 (inv\_d2, d[2]);

not not1 (inv\_d1, d[1]);

not not0 (inv\_d0, d[0]);

or or1(in, inv\_d1, inv\_d0);

and out(l, in, inv\_d2);

endmodule

module tb\_p2();

reg[2:0] d;

wire l;

integer i;

p2 UUT (l, d);

initial

begin

#10 $monitor("D = %b", d, ", L = ", l);

for( i = 0; i <= 7; i = i + 1)

begin

d = i;

#10

$display("\n\n");

end

end

endmodule

